What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory array in which a plurality of memory cells are two-dimensionally arranged;

a selecting circuit which selects one of the memory cell from the memory array;

a storage device in which a sequence for controlling write and erase operations for the memory cells is stored; and

a power generator which is able to generate certain voltage higher than requirement voltage for write or erase operation;

a connecting circuit which connects the selecting circuit with the power generator; and

a write or erase controller for reading the sequence from the storage unit to control the write and erase operations for the memory cells,

wherein the sequence includes a plurality of sub-sequences in which write or erase operation to the memory cell is implemented,

wherein each of the sub-sequences includes before the end of the sub-sequence:

a voltage resetting step of resetting a voltage impressed on the selecting circuit to the power voltage or grounding; and

a route resetting step of resetting a switch of a transistor of the selecting circuit to last status just before write or erase operation.

2. A nonvolatile semiconductor memory device according to claim 1, wherein the sequence has the plurality of sub-sequences which are sequentially arranged, and further includes the skip check step of checking whether the

sub-sequences are skipped or not before the start of the sub-sequences.

3. A nonvolatile semiconductor memory device according to claim 2, wherein the skip check step checks whether the sub-sequences are skipped or not by using flags which are stored in the write or erase controller in advance.

4. A nonvolatile semiconductor memory device according to claim 1, wherein the sequence further includes the suspend step of checking whether execution of the sequence is temporarily stopped or not between two adjacent sub-sequences.

5. A nonvolatile semiconductor memory device according to claim 1, wherein the sub-sequence includes the step of checking whether verification for deciding levels which the memory cells reach in a write or erase operation is passed or not.